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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/742,327	12/18/2003	Ely K. Tsern	60809-0146-US	5522
38426	7590	04/05/2007	EXAMINER	
MORGAN LEWIS & BOCKIUS LLP/RAMBUS INC. 2 PALO ALTO SQUARE 3000 EL CAMINO REAL PALO ALTO, CA 94306			CHEUNG, MARY DA ZHI WANG	
			ART UNIT	PAPER NUMBER
			3694	
SHORTENED STATUTORY PERIOD OF RESPONSE		MAIL DATE	DELIVERY MODE	
3 MONTHS		04/05/2007	PAPER	

Please find below and/or attached an Office communication concerning this application or proceeding.

If NO period for reply is specified above, the maximum statutory period will apply and will expire 6 MONTHS from the mailing date of this communication.

<b>Office Action Summary</b>	<b>Application No.</b>	<b>Applicant(s)</b>	
	10/742,327	TSERN ET AL.	
	<b>Examiner</b>	<b>Art Unit</b>	
	Mary Cheung	3694	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --  
**Period for Reply**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

#### Status

1) Responsive to communication(s) filed on 23 January 2007.  
 2a) This action is **FINAL**.                  2b) This action is non-final.  
 3) Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

#### Disposition of Claims

4) Claim(s) 16-54 and 62-69 is/are pending in the application.  
 4a) Of the above claim(s) \_\_\_\_\_ is/are withdrawn from consideration.  
 5) Claim(s) 24-36,41-54 and 62-69 is/are allowed.  
 6) Claim(s) 16-22 and 37-40 is/are rejected.  
 7) Claim(s) \_\_\_\_\_ is/are objected to.  
 8) Claim(s) \_\_\_\_\_ are subject to restriction and/or election requirement.

#### Application Papers

9) The specification is objected to by the Examiner.  
 10) The drawing(s) filed on \_\_\_\_\_ is/are: a) accepted or b) objected to by the Examiner.  
     Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).  
     Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).  
 11) The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

#### Priority under 35 U.S.C. § 119

12) Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).  
 a) All    b) Some \* c) None of:  
 1. Certified copies of the priority documents have been received.  
 2. Certified copies of the priority documents have been received in Application No. \_\_\_\_\_.  
 3. Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

\* See the attached detailed Office action for a list of the certified copies not received.

#### Attachment(s)

1) <input type="checkbox"/> Notice of References Cited (PTO-892)	4) <input type="checkbox"/> Interview Summary (PTO-413)
2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948)	Paper No(s)/Mail Date. _____
3) <input type="checkbox"/> Information Disclosure Statement(s) (PTO/SB/08)	5) <input type="checkbox"/> Notice of Informal Patent Application
Paper No(s)/Mail Date _____	6) <input type="checkbox"/> Other: _____

## **DETAILED ACTION**

### ***Status of the Claims***

1. This action is in response to the amendment filed on January 23, 2007. Claims 16-22, 24-54 and 62-69 are pending. Claims 1-15, 23 and 55-61 are canceled. Claims 62-69 are added. Claims 16 and 32 are amended. After reviewing the applicant's request for reinstating the withdrawn claims 32-36 and 45-54 since claim 24 is generic to these claims, claims 32-36 and 45-54 are reinstated at this time. Thus, all the pending claims are examined.

### ***Response to Arguments***

2. Applicant's arguments filed January 23, 2007 have been fully considered but they are not persuasive.

In response to the applicant's arguments that the combination of Dieffenderfer (U. S. Patent 5,910,930) and Foss (U. S. Patent 5,796,673) would not likely to succeed because the two references are not incompatible since the Dieffenderfer uses a microprocessor to select power mode, and the integrated circuit disclosed in Foss is a memory not a microprocessor, examiner respectfully disagrees. Dieffenderfer teaches using a delay locked loop to control the clock signals for selecting power mode (column 4 lines 45-51). Foss teaches a clock control signals circuit integrated in a single integrated circuit chip, and the device is not limited for use in conjunctions with various types of memory device but also other designs of the delay locked loop (column 4 lines 41-48 and column 6 claim 6). Thus, the Foss's teaching is compatible with Dieffenderfer's teaching.

In response to applicant's argument that lack of motivation to combine the teachings of Dieffenderfer and Foss, examiner respectfully disagrees because both of the references deal with using delay locked loop to control clock signals (Dieffenderfer: column 4 liens 45-51; Foss: column 4 lines 4-16, 41-48).

***Claim Rejections - 35 USC § 103***

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

4. Claims 16-22 and 37-40 are rejected under 35 U.S.C. 103(a) as being unpatentable over Dieffenderfer et al., U. S. Patent 5,910,930 in view of Foss et al., U. S. Patent 5,796,673.

As to claim 16, Dieffenderfer teaches a memory device having a core that includes memory cells, the memory device comprising (Fig. 1):

- a) A core that includes dynamic random access memory cells (column 3 line 59 – column 4 line 14);
- b) A clock receiver circuit to receive an external clock signal (column 3 line 59 – column 4 line 14 and Fig. 1);
- c) A delay locked loop circuit coupled to the clock receiver circuit, wherein (column 4 lines 45-51 and Fig. 1);
- d) During a first power mode the delay locked loop circuit and the clock receiver circuit are turned on (column 4 lines 45-49 and column 5 lines 4-6); wherein

power consumption is the first power mode is less than that consume while in an active mode (column 1 lines 14-17, 62-65 and column 3 lines 35-41);

- e) During a second power mode, the delay locked circuit is turned off (column 5 lines 1-3, 17-21).

Dieffenderfer does not teach the memory device is a single chip dynamic random access memory device. However, Foss teaches this matter (column 4 line 4 – column 6 line 37; specifically, column 6 claim 6 in Foss' teaching). It would have been obvious to one of ordinary skill in the art at the time the invention was made to allow the memory cells, the clock receiver circuit, and the delay locked loop in Dieffenderfer's teaching to be integrated into a single memory chip as taught by Foss for simplification of the device.

As to claim 17, Dieffenderfer teaches the second power mode is a power down mode (column 5 lines 1-3, 17-21).

As to claim 18, Dieffenderfer teaches during the second power mode, the clock receiver circuit is turned off (column 5 lines 1-3, 17-21).

As to claim 19, Dieffenderfer teaches a first control line, coupled to the clock receiver circuit and the delay locked loop circuit, wherein, during the second power mode, the delay locked loop circuit and the clock receiver circuit are turned off using the first control line (column 4 line 45 – column 5 line 39 and Fig. 1).

As to claims 20-21, Dieffenderfer teaches wherein during a third power mode, the delay locked loop circuit is in a low power configuration and the clock receiver circuit is turned on (column 4 lines 60-61).

As to claims 22 and 40, Dieffenderfer teaches a resynchronization time of the delay locked loop circuit in the low power configuration is less than a resynchronization time of the delay locked loop circuit in the second power mode or the power down mode (column 5 lines 6-8, 19-21).

As to claim 37, Dieffenderfer teaches a method of operation of a memory device having a core of dynamic random access memory cells, a delay locked loop circuit, and a clock receiver circuit coupled to the delay locked loop circuit the method comprising (column 3 line 59 – column 4 line 14 and Fig. 1):

- a) Receiving a command that specifies a power down mode (column 4 lines 52-56);
- b) Turning off a delay locked loop circuit in response to the command that specifies the power down mode (column 5 lines 1-3, 17-21);
- c) Operating the memory device in a standby power mode, wherein the delay locked loop circuit and the clock receiver circuit are turned on in the standby mode (column 4 lines 45-49 and column 5 lines 4-6).

Dieffenderfer does not teach the memory device is a single chip dynamic random access memory device. However, Foss teaches this matter (column 4 line 4 – column 6 line 37; specifically, column 6 claim 6 in Foss' teaching). It would have been obvious to one of ordinary skill in the art at the time the invention was made to allow the memory cells, the clock receiver circuit, and the delay locked loop in Dieffenderfer's teaching to be integrated into a single memory chip as taught by Foss for simplification of the device.

As to claim 38, Dieffenderfer teaches wherein during the power down mode, the clock receiver circuit is turned off (column 5 lines 1-3, 17-21).

As to claim 39, Dieffenderfer teaches operating the memory device in a nap mode, wherein during the nap mode, the delay locked loop circuit is in a low power configuration and the clock receiver circuit is on (column 4 lines 60-61).

***Allowable Subject Matter***

5. Claims 24-36, 41-54 and 62-69 are allowed.

***Conclusion***

6. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

***Inquire***

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Mary Cheung whose telephone number is (571)-272-6705. The examiner can normally be reached on Monday – Thursday from 10:00 AM to

7:00 PM. If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, James Trammell, can be reached on (571) 272-6712.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

The fax phone number for the organization where this application or proceedings is assigned are as follows:

(571) 273-8300 (Official Communications; including After Final Communications labeled "BOX AF")

(571) 273-6705 (Draft Communications)

Mary Cheung  
March 28, 2007



MARY D. CHEUNG  
PRIMARY EXAMINER